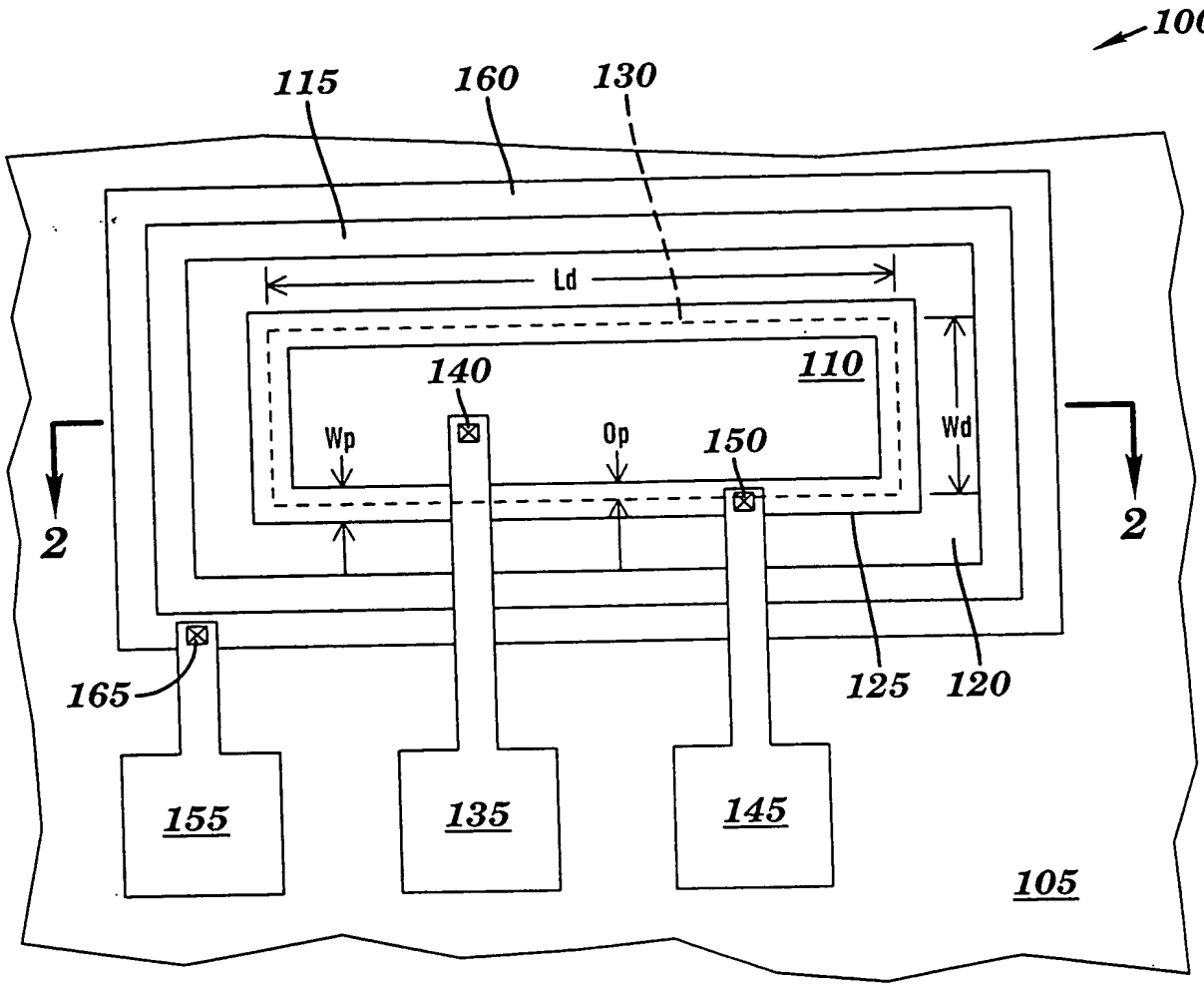
100
115
160
130
Ld
140
110
Wp
Op
150
Wd
2
2
165
125
120
155
135
145
105

FIG. 1

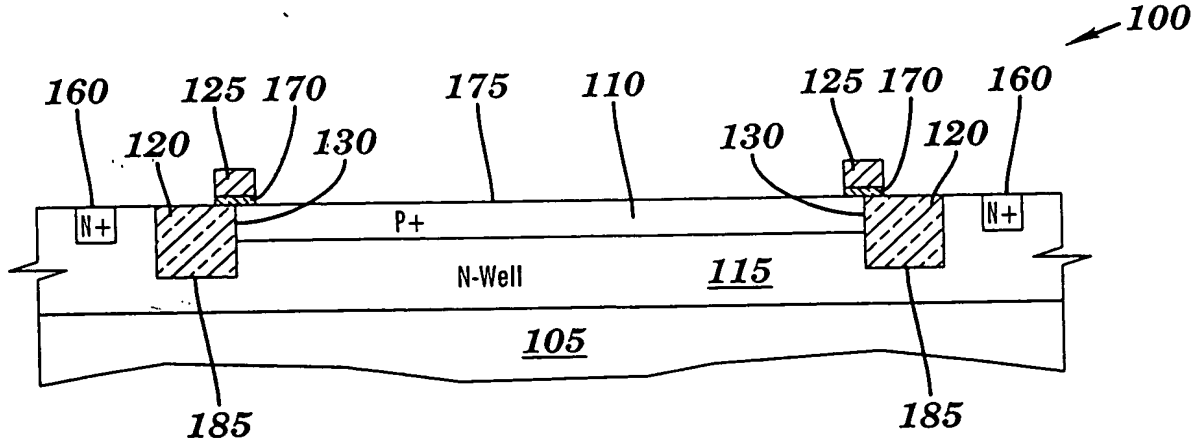
100
160
125
170
175
110
125
170
160
120
130
130
120
N+
P+
N+
N-Well
115
105
185
185

FIG. 2

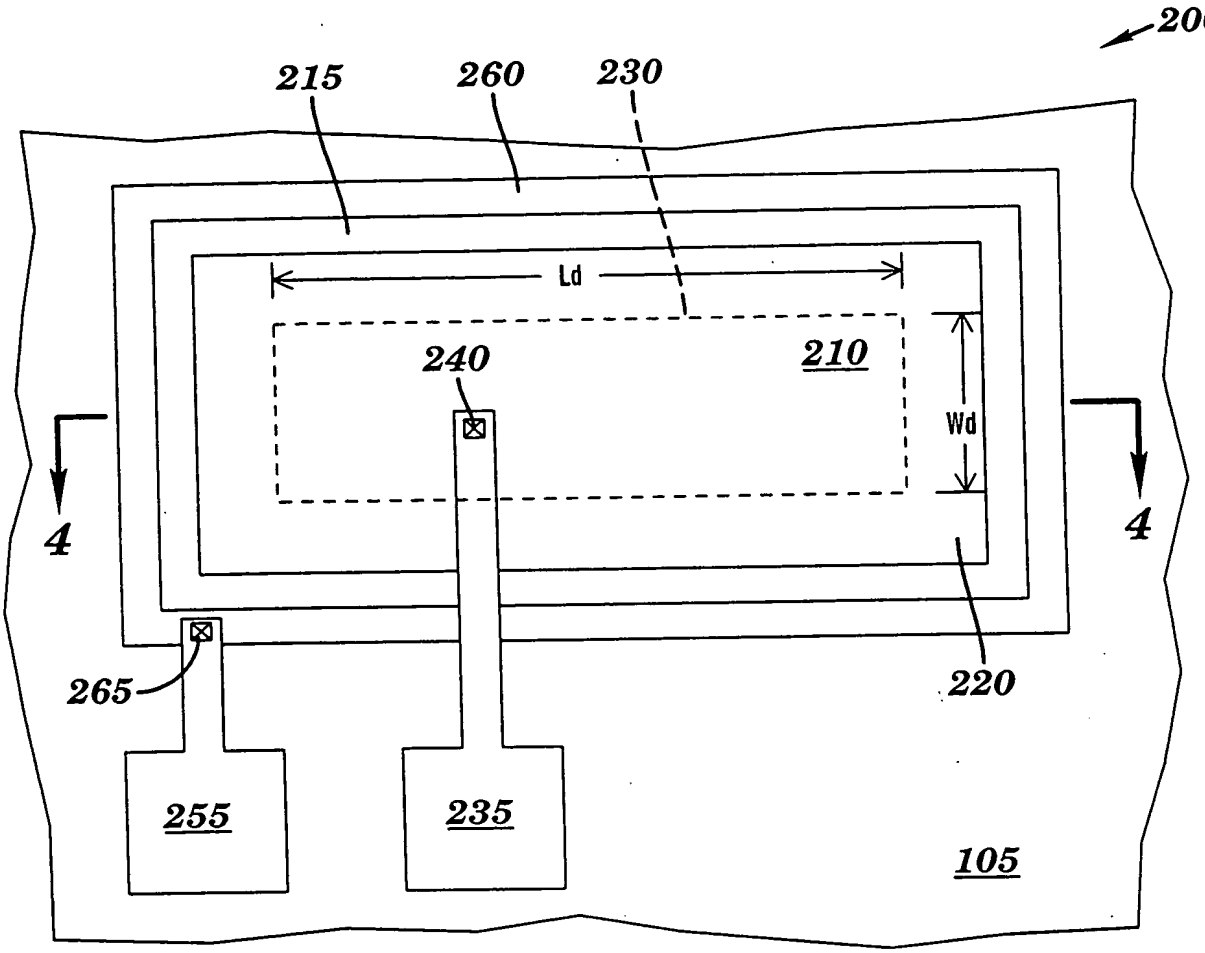
200
215
260
230
Ld
240
210
Wd
4
4
265
220
255
235
105

FIG. 3

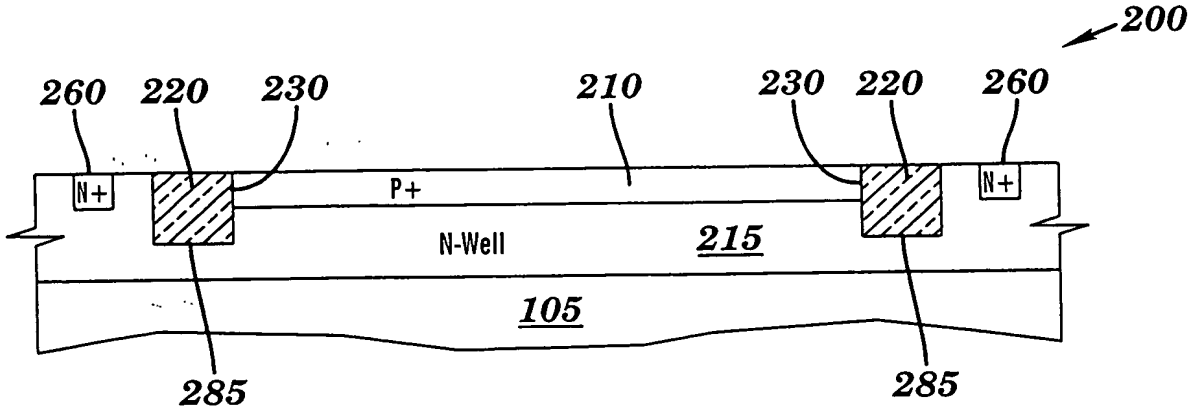
200
260
220
230
210
230
220
260
N+
P+
N+
N-Well
215
105
285
285

FIG. 4

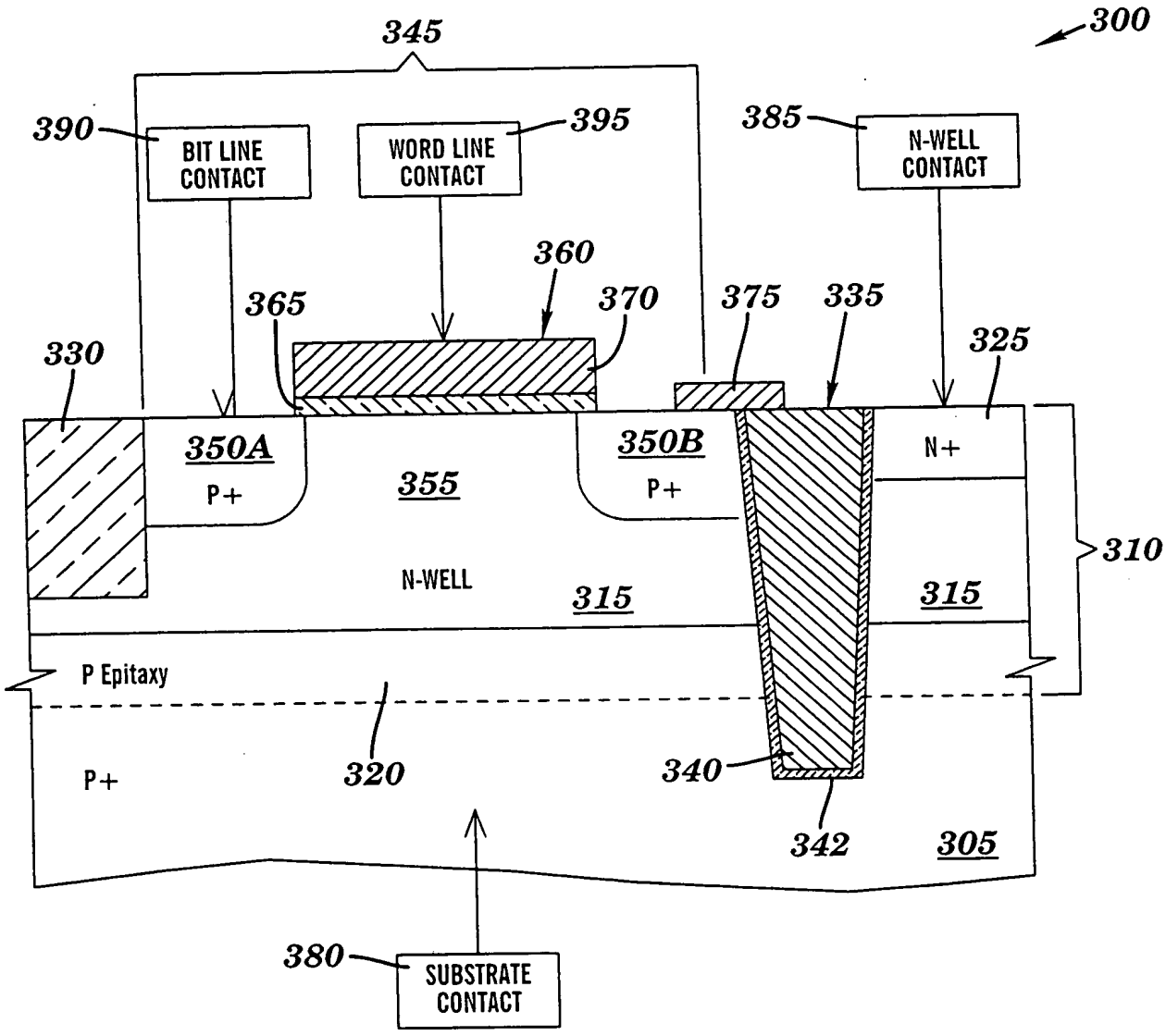
300
345
390
BIT LINE CONTACT
395
WORD LINE CONTACT
385
N-WELL CONTACT
360
365
370
375
335
325
330
350A
P+
355
350B
P+
N+
310
N-WELL
315
315
P Epitaxy
320
340
342
305
P+
380
SUBSTRATE CONTACT

FIG. 5

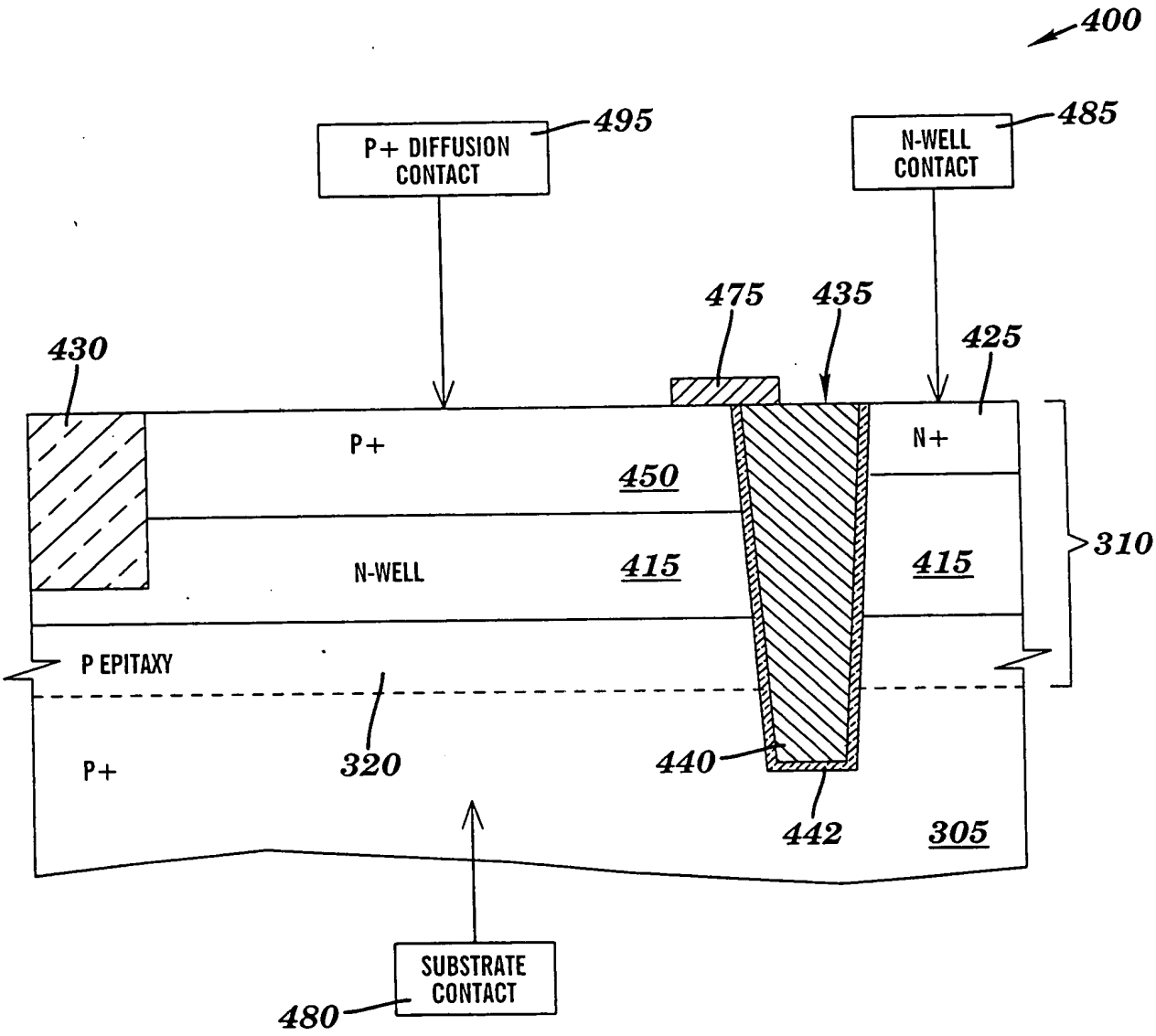
400
P+ DIFFUSION CONTACT
495
N-WELL CONTACT
485
475
435
425
430
P+
450
N+
N-WELL
415
415
310
P EPITAXY
320
440
442
305
P+
SUBSTRATE CONTACT
480

FIG. 6

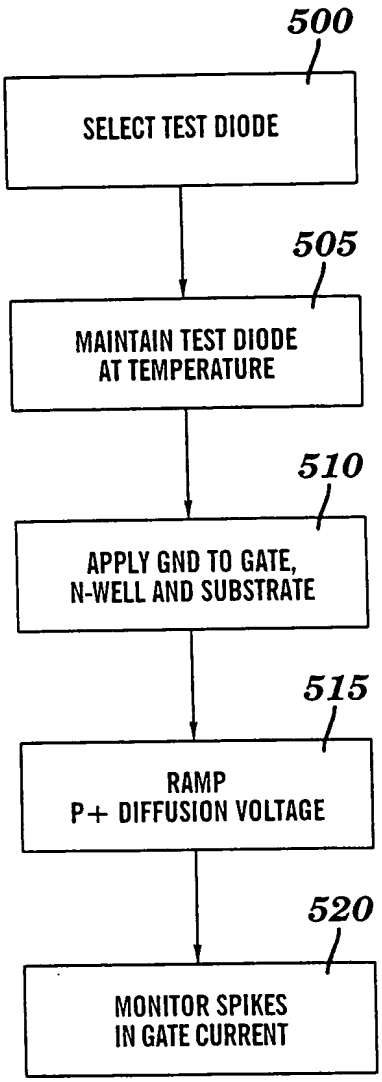

FIG. 7A

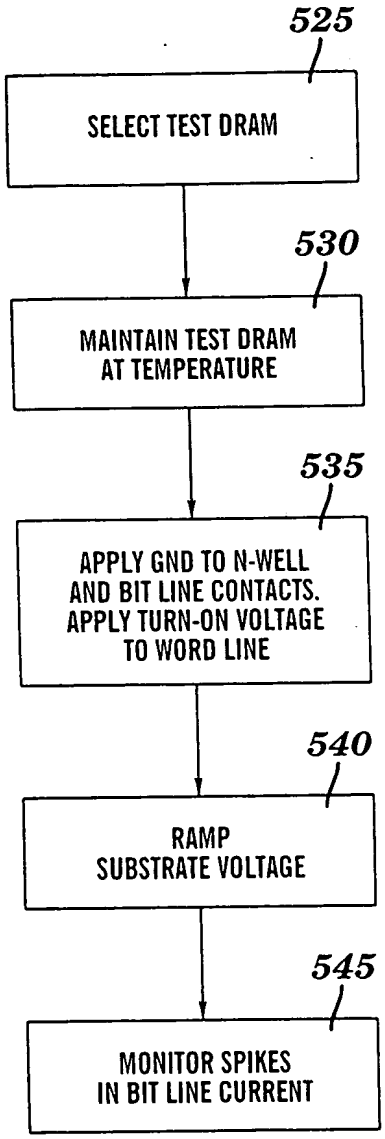

FIG. 7B

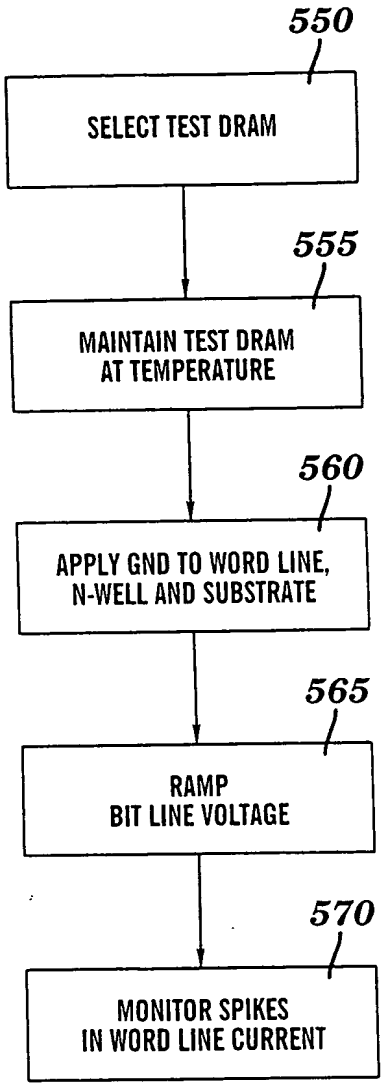

FIG. 7C

P+ POLYSILICON-BOUNDED DIODE WITHOUT STRESS-INDUCED DEFECTS

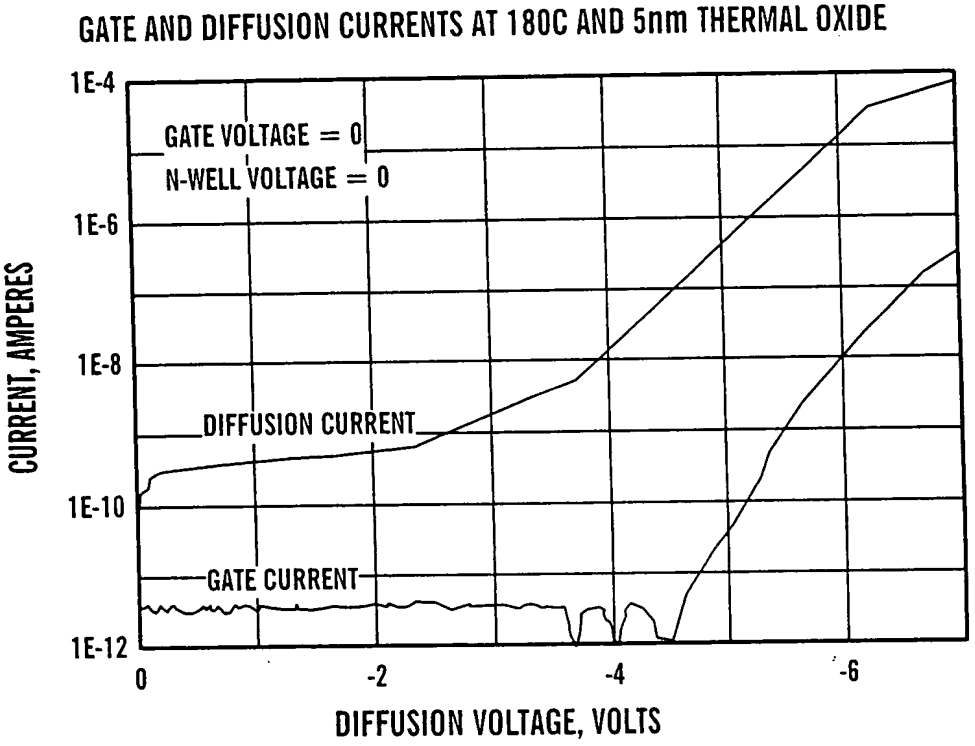

FIG. 8

P+ POLYSILICON-BOUNDED DIODE WITH STRESS-INDUCED DEFECTS

GATE AND DIFFUSION CURRENTS AT 180C AND 5nm THERMAL OXIDE

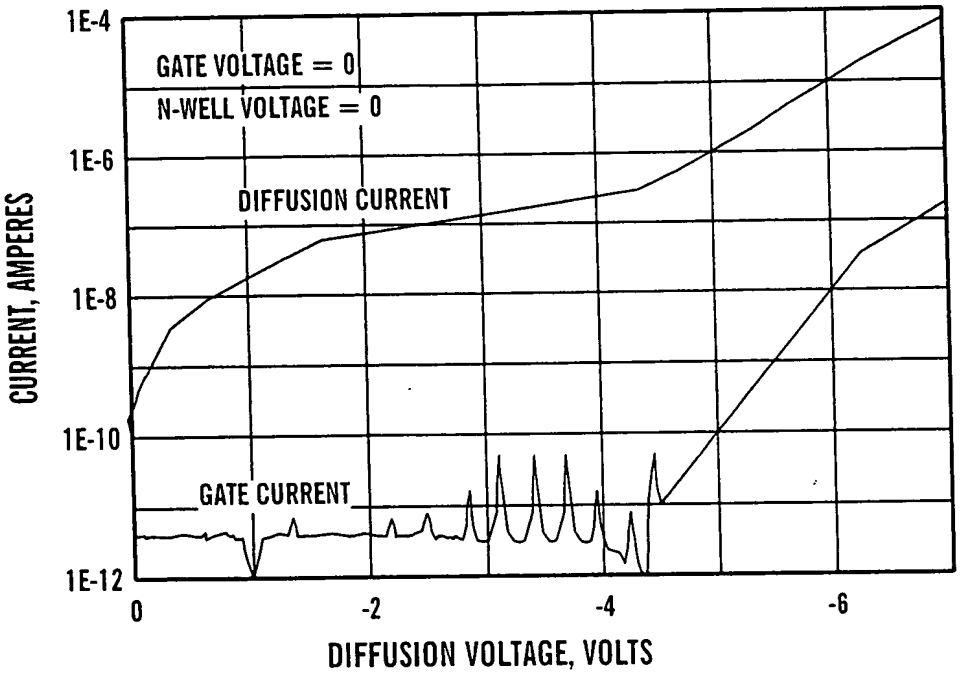

FIG. 9

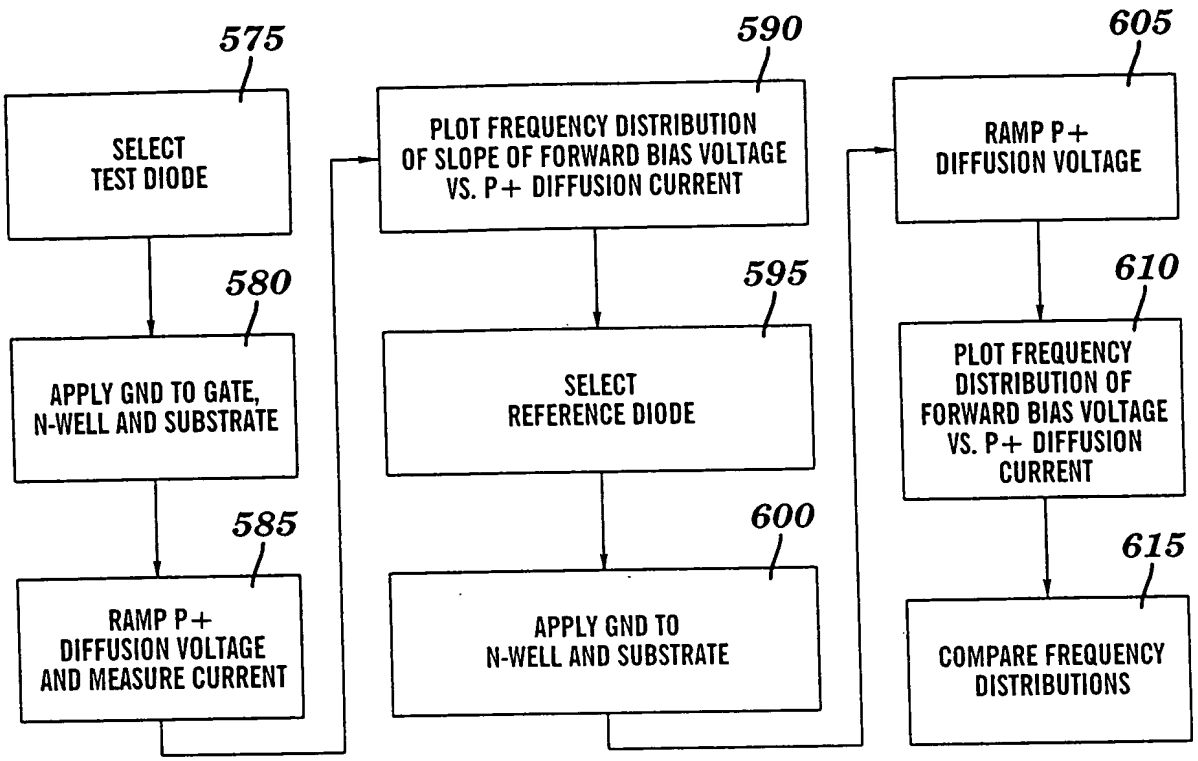

FIG. 10A

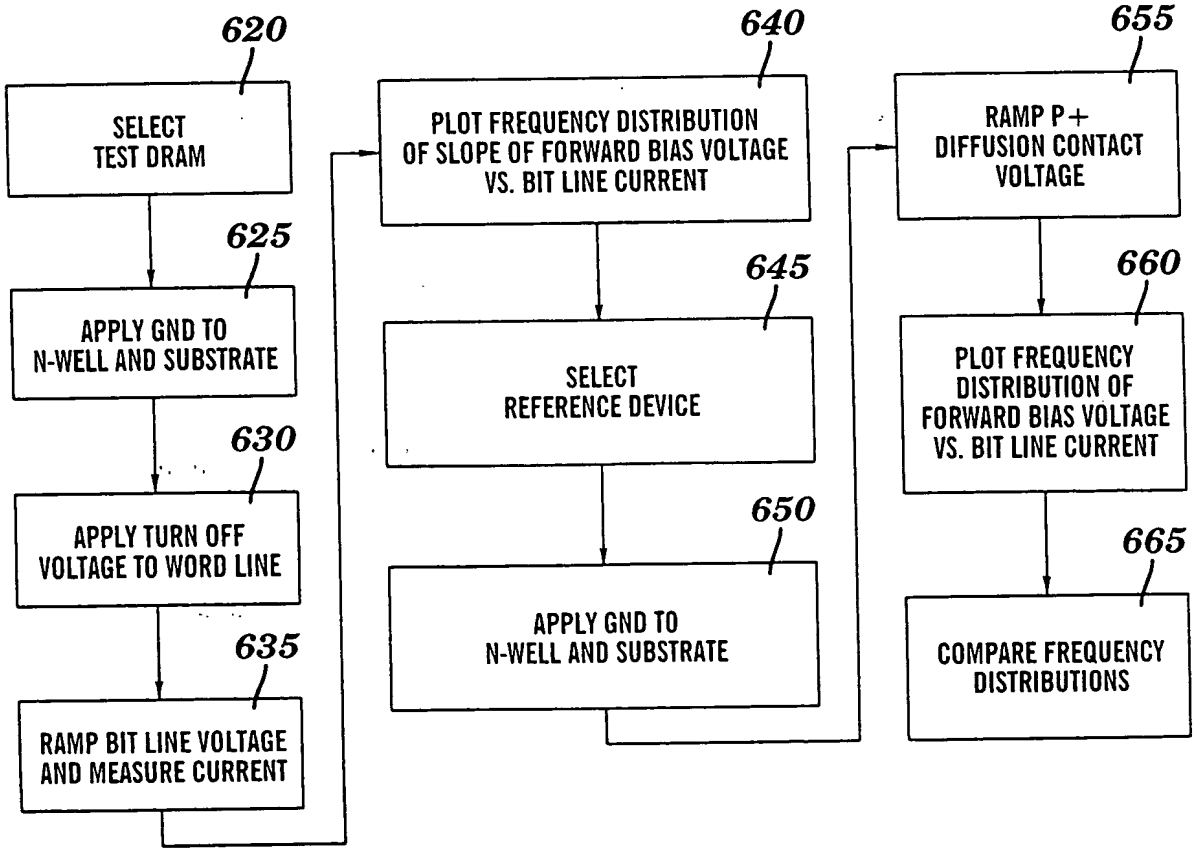

FIG. 10B

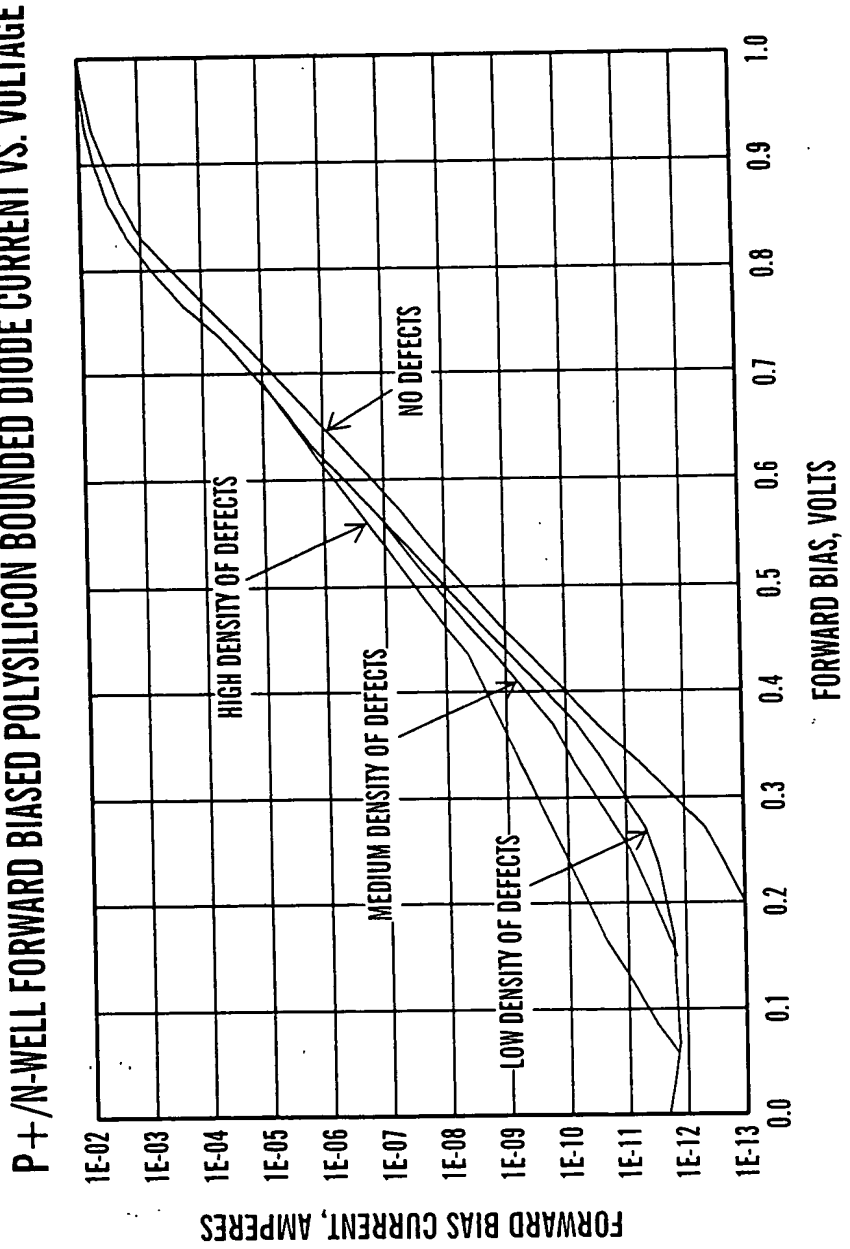
P+/N-WELL FORWARD BIASED POLYSILICON BOUNDED DIODE CURRENT VS. VOLTAGE
FORWARD BIAS CURRENT, AMPERES
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
FORWARD BIAS, VOLTS
HIGH DENSITY OF DEFECTS
MEDIUM DENSITY OF DEFECTS
LOW DENSITY OF DEFECTS
NO DEFECTS

FIG. 11

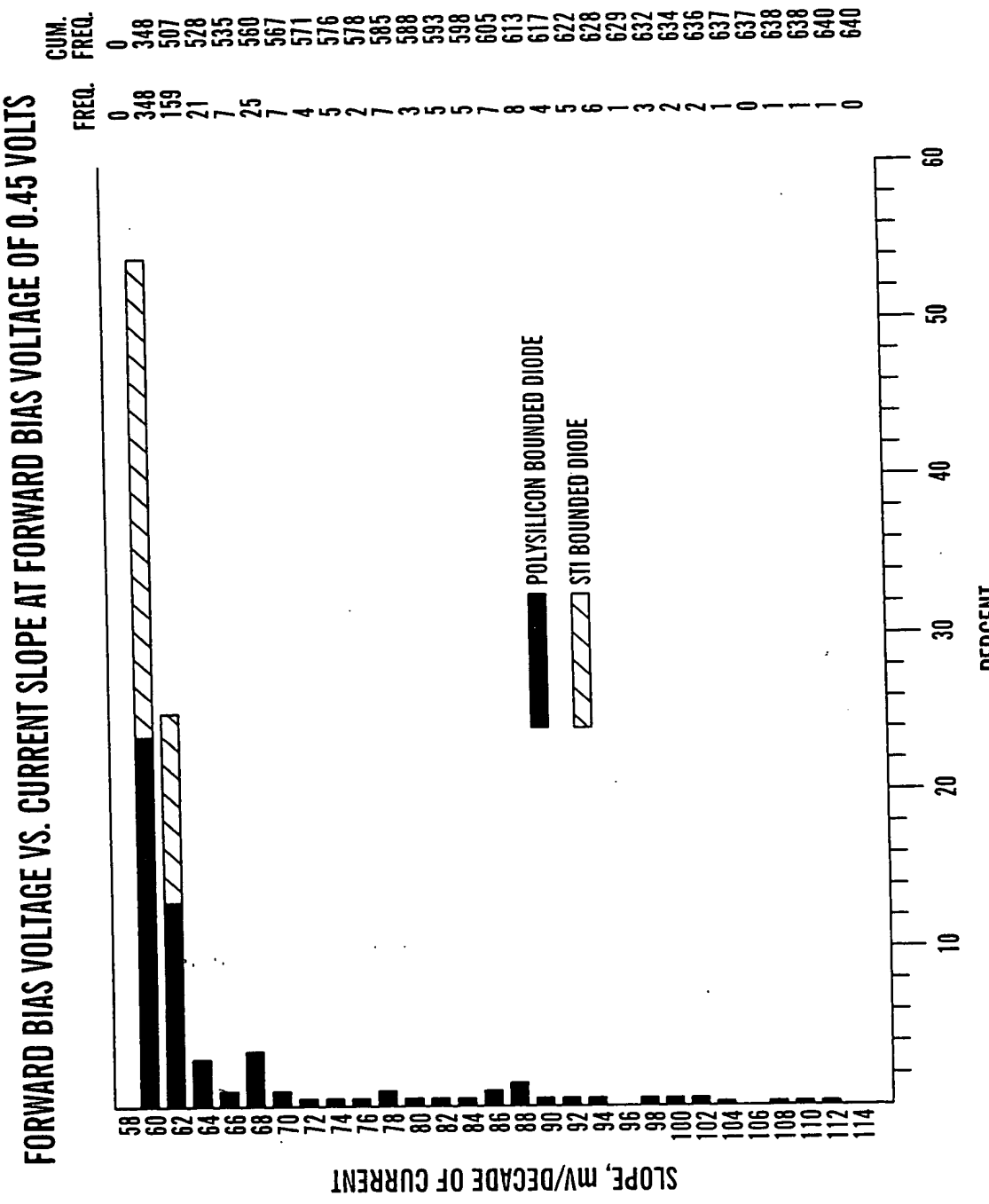
FORWARD BIAS VOLTAGE VS. CURRENT SLOPE AT FORWARD BIAS VOLTAGE OF 0.45 VOLTS
FREQ.
CUM. FREQ.
0 0
348 348
159 507
21 528
7 535
25 560
7 567
4 571
5 576
2 578
7 585
3 588
5 593
5 598
7 605
8 613
4 617
5 622
6 628
1 629
3 632
2 634
2 636
1 637
0 637
1 638
1 638
1 640
0 640
58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98 100 102 104 106 108 110 112 114
SLOPE, mV/DECADE OF CURRENT
POLYSILICON BOUNDED DIODE
STI BOUNDED DIODE
10 20 30 40 50 60
PERCENT

FIG. 12

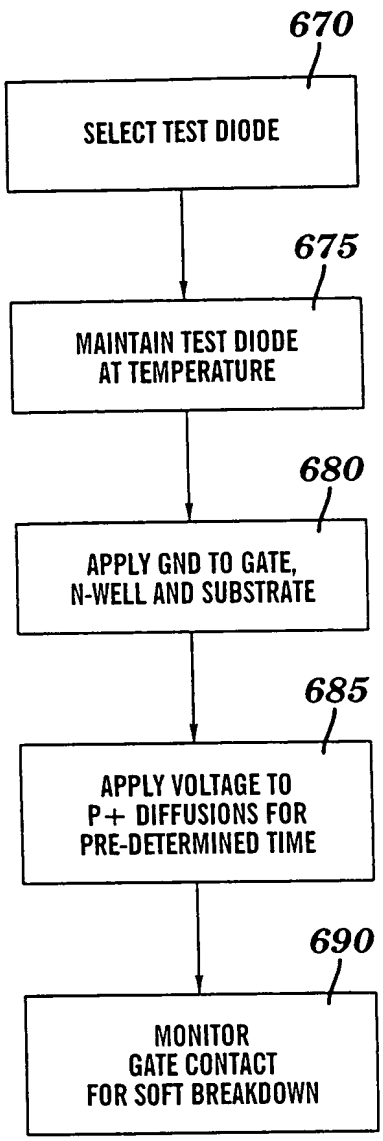

FIG. 13A

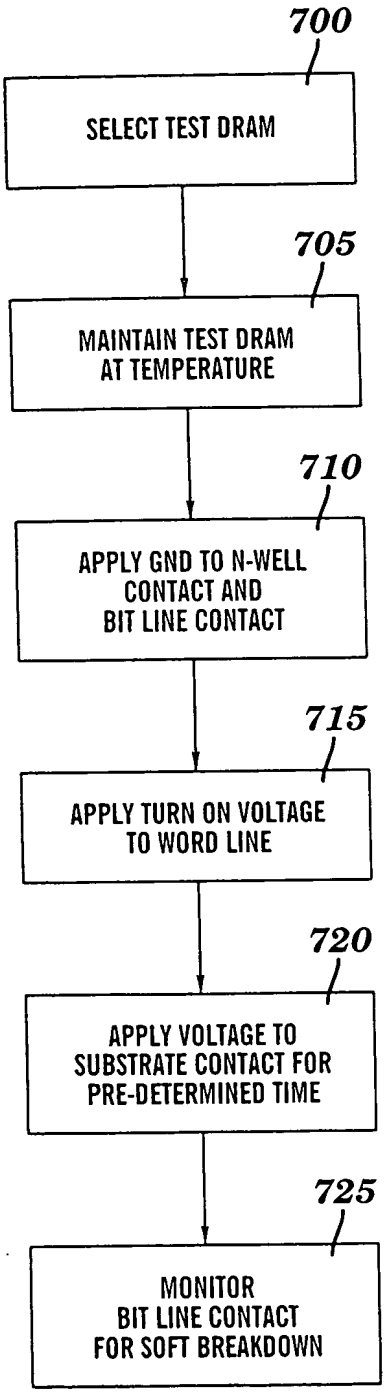

FIG. 13B

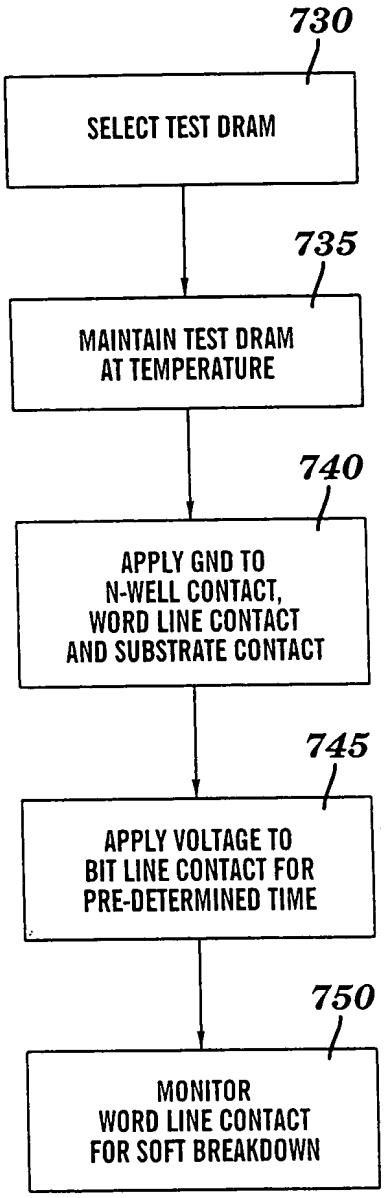

FIG. 13C

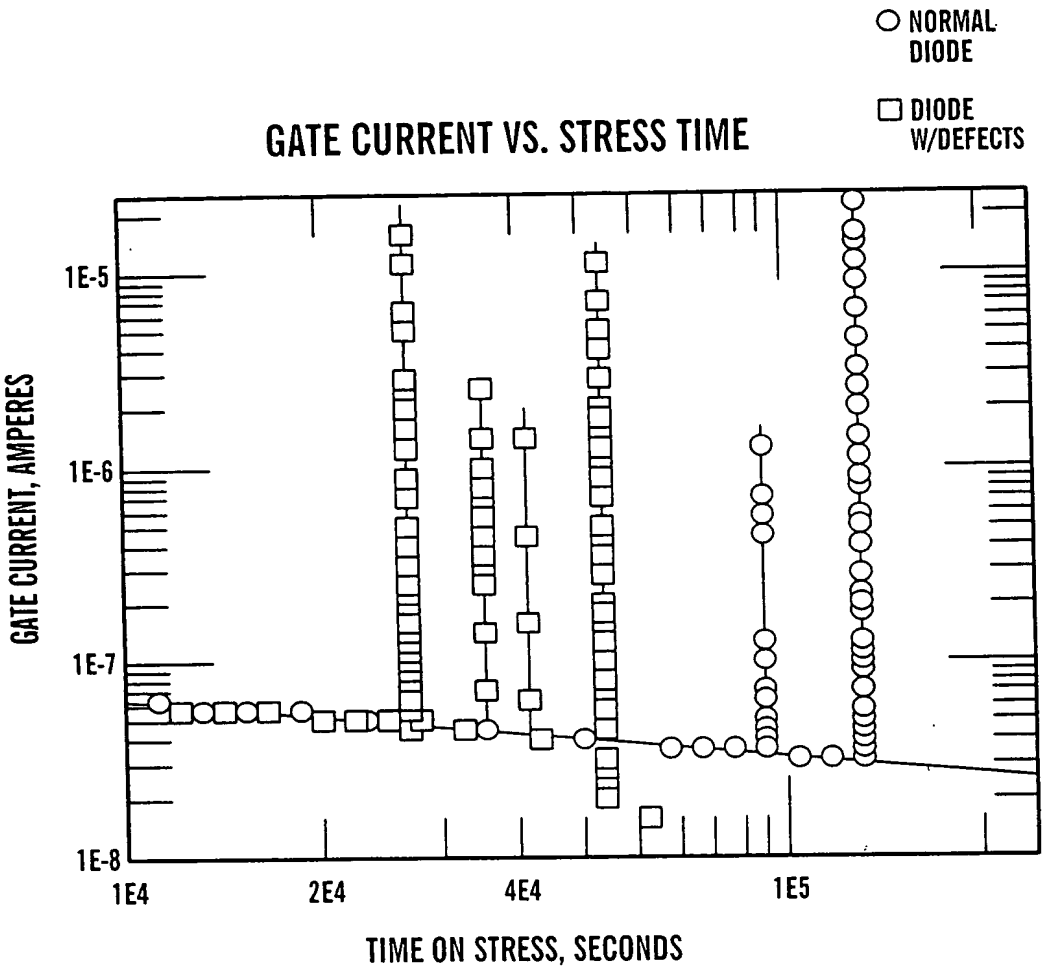
NORMAL DIODE
DIODE W/DEFECTS
GATE CURRENT VS. STRESS TIME
GATE CURRENT, AMPERES
1E-5
1E-6
1E-7
1E-8
1E4
2E4
4E4
1E5
TIME ON STRESS, SECONDS

FIG. 14

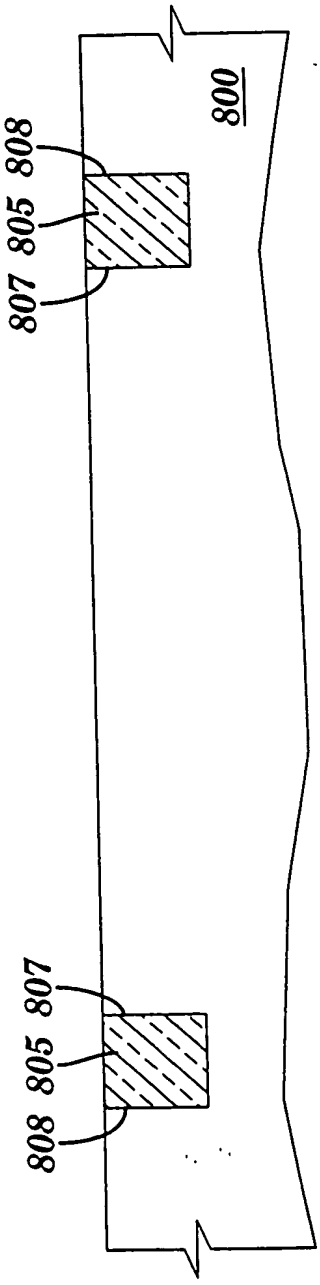

FIG. 15A

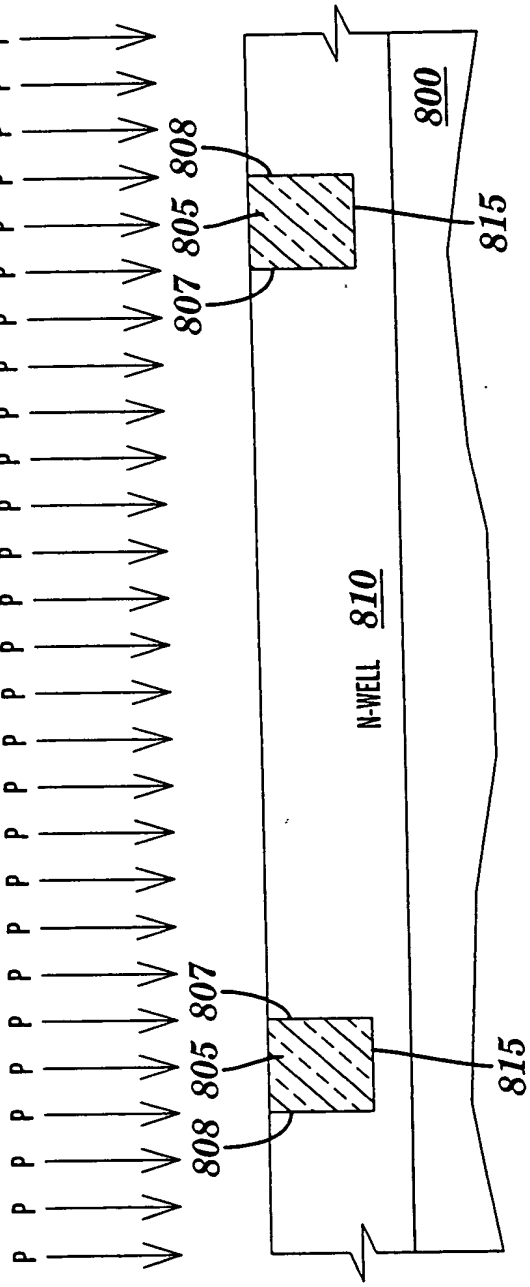

FIG. 15B

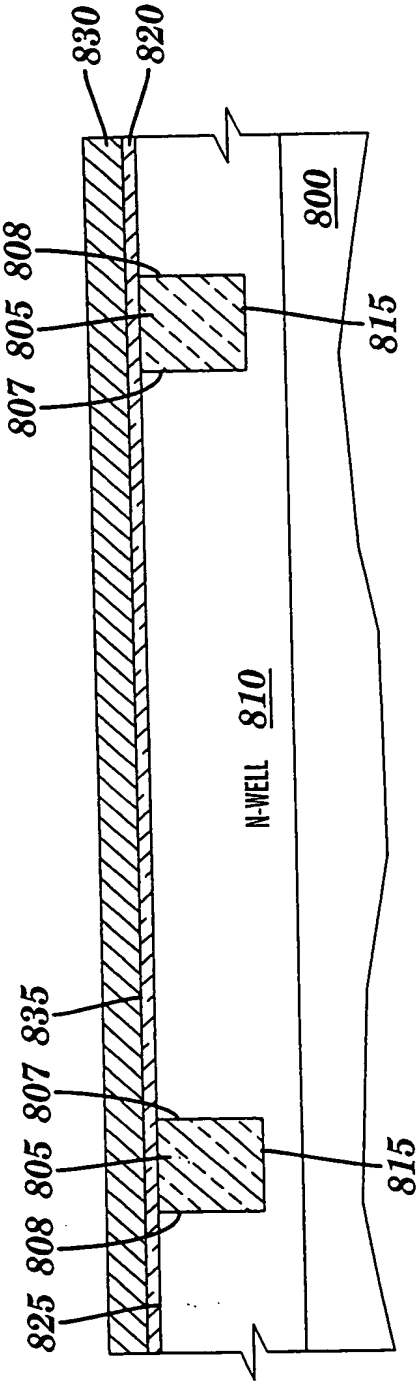

FIG. 15C

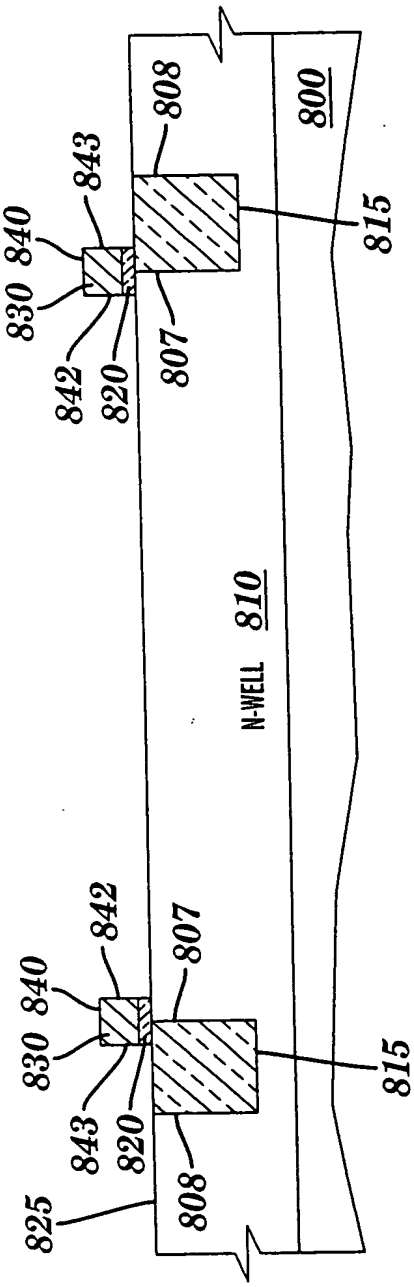

FIG. 15D

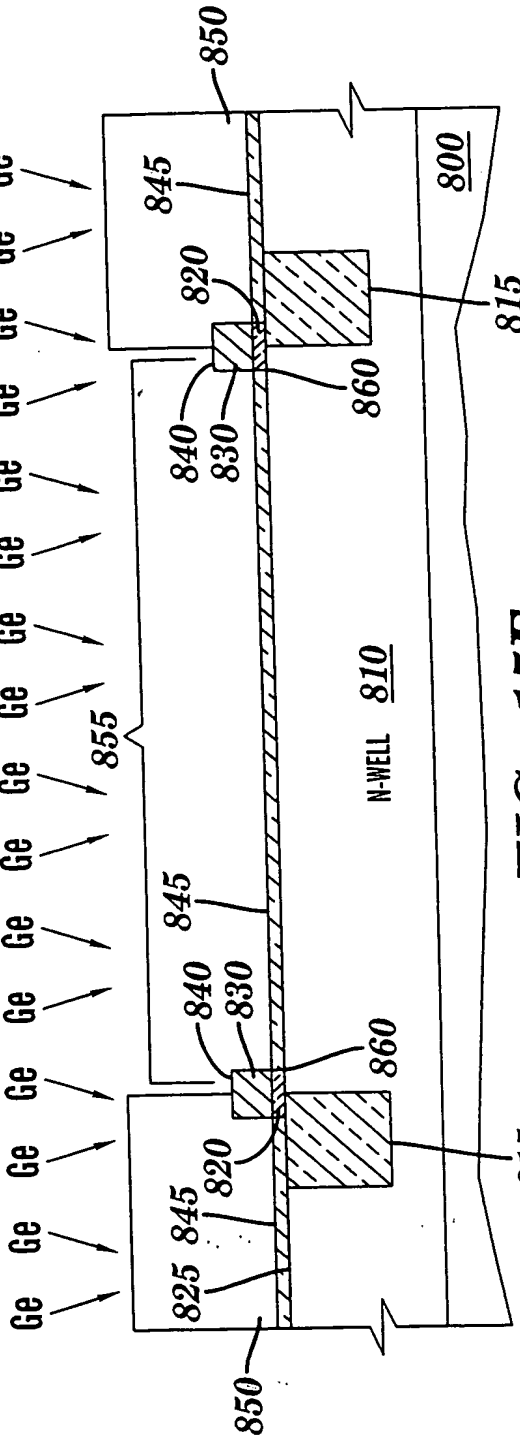

FIG. 15E

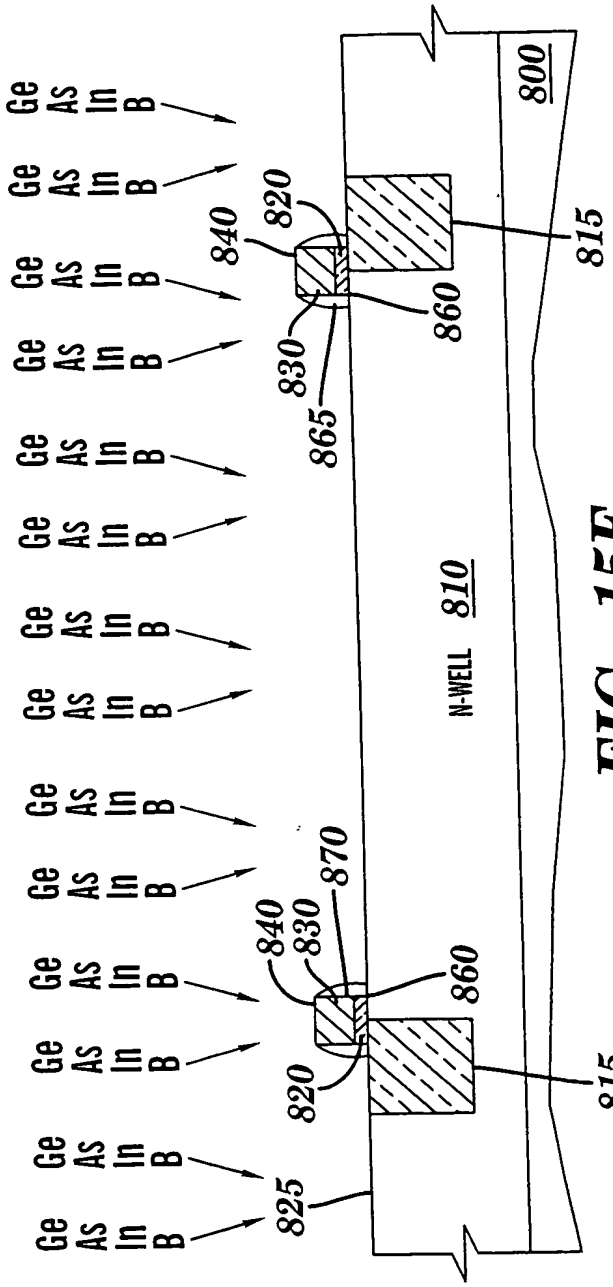

FIG. 15F

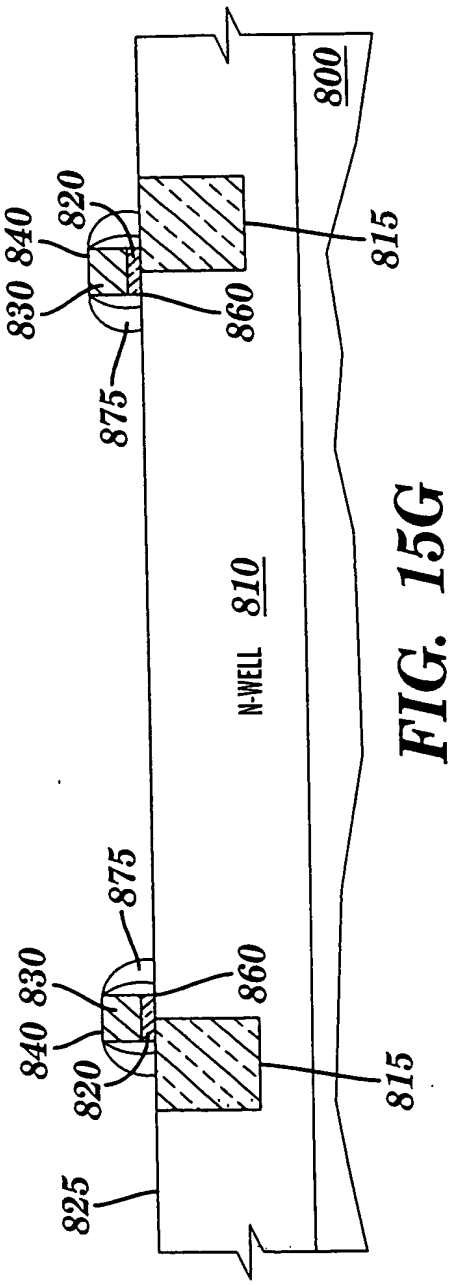

FIG. 15G

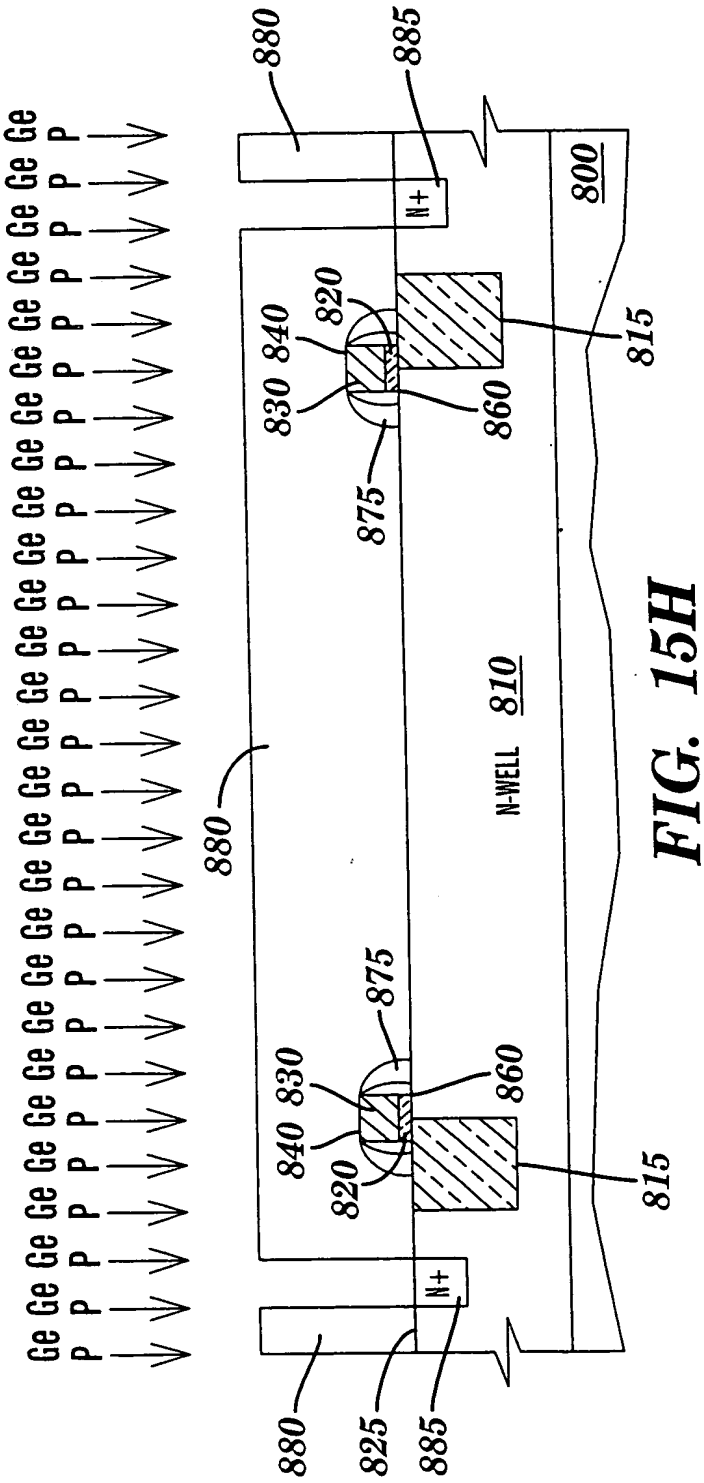

FIG. 15H

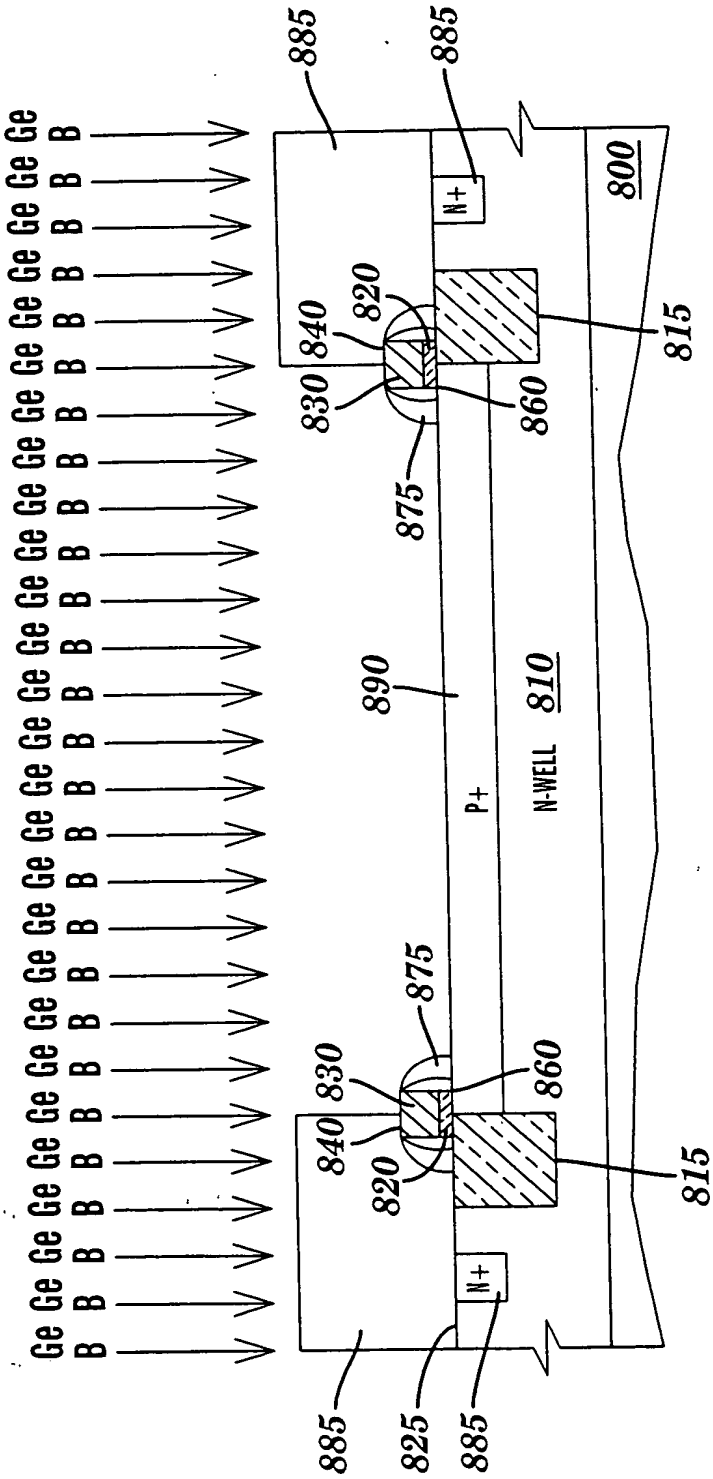

FIG. 15I

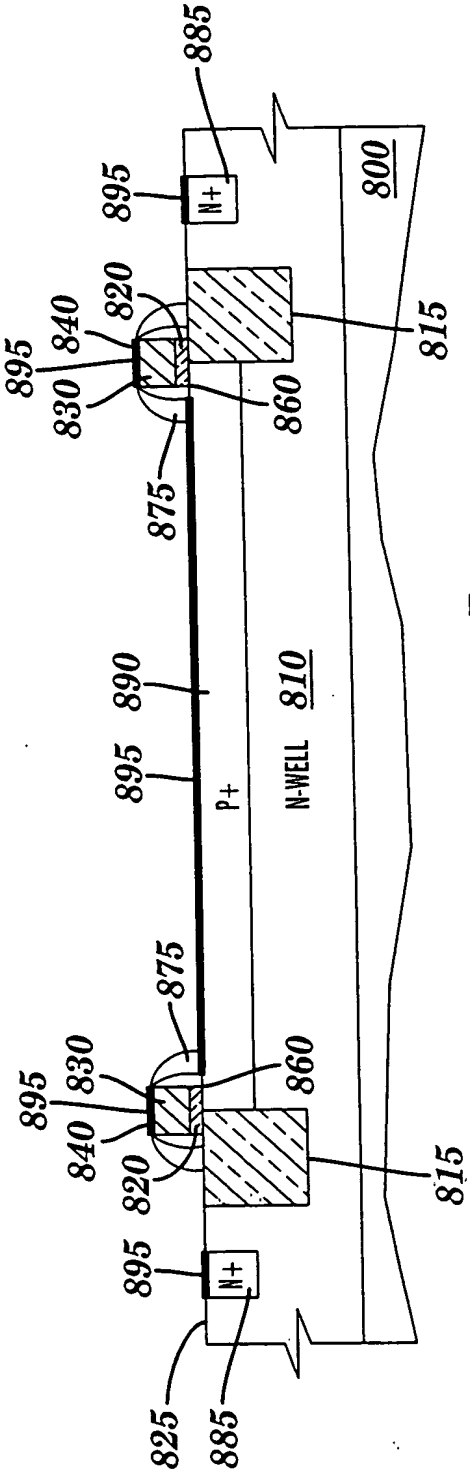

FIG. 15J

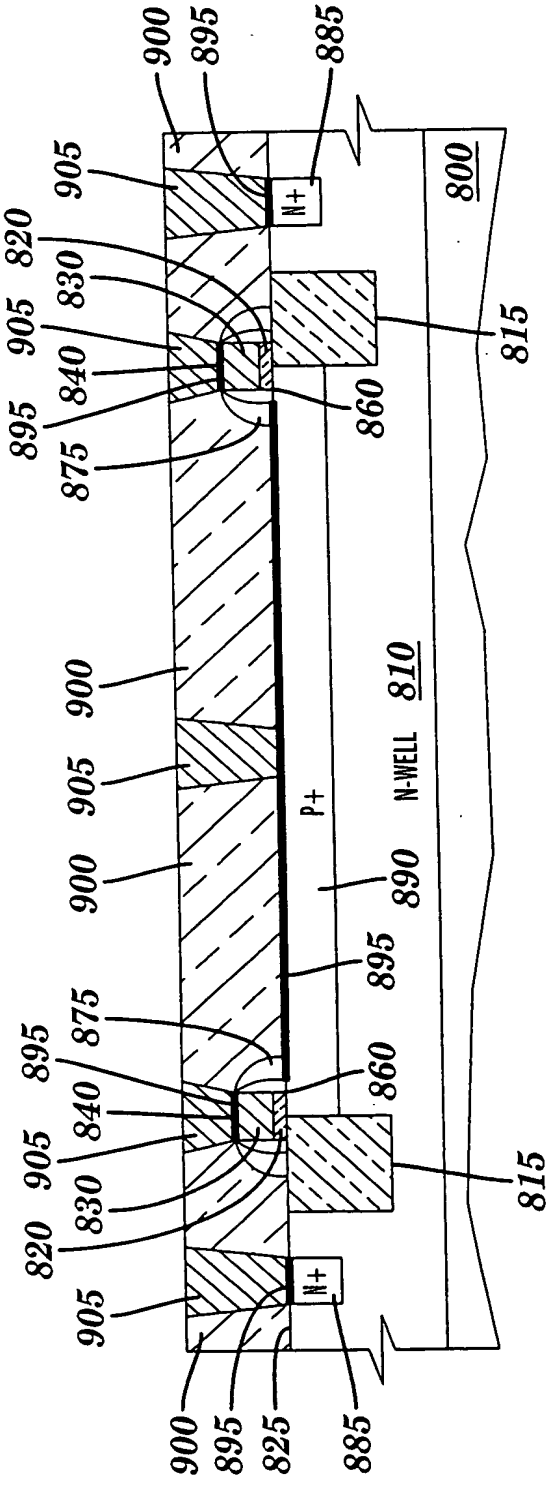

FIG. 15K

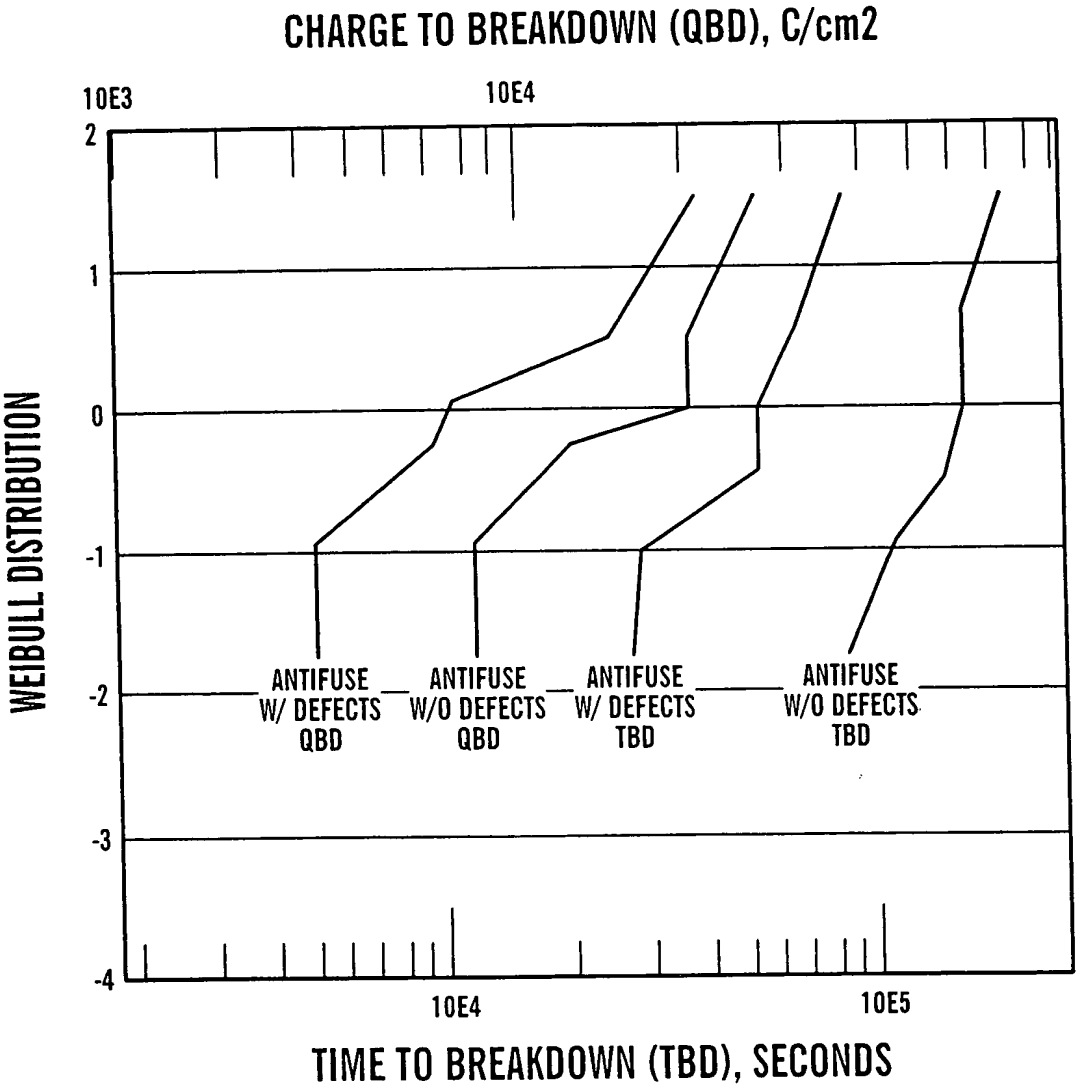
CHARGE TO BREAKDOWN (QBD), C/cm2
10E3
10E4
2
1
0
-1
-2
-3
-4
WEIBULL DISTRIBUTION
ANTIFUSE W/ DEFECTS QBD
ANTIFUSE W/O DEFECTS QBD
ANTIFUSE W/ DEFECTS TBD
ANTIFUSE W/O DEFECTS TBD
10E4
10E5
TIME TO BREAKDOWN (TBD), SECONDS

FIG. 16

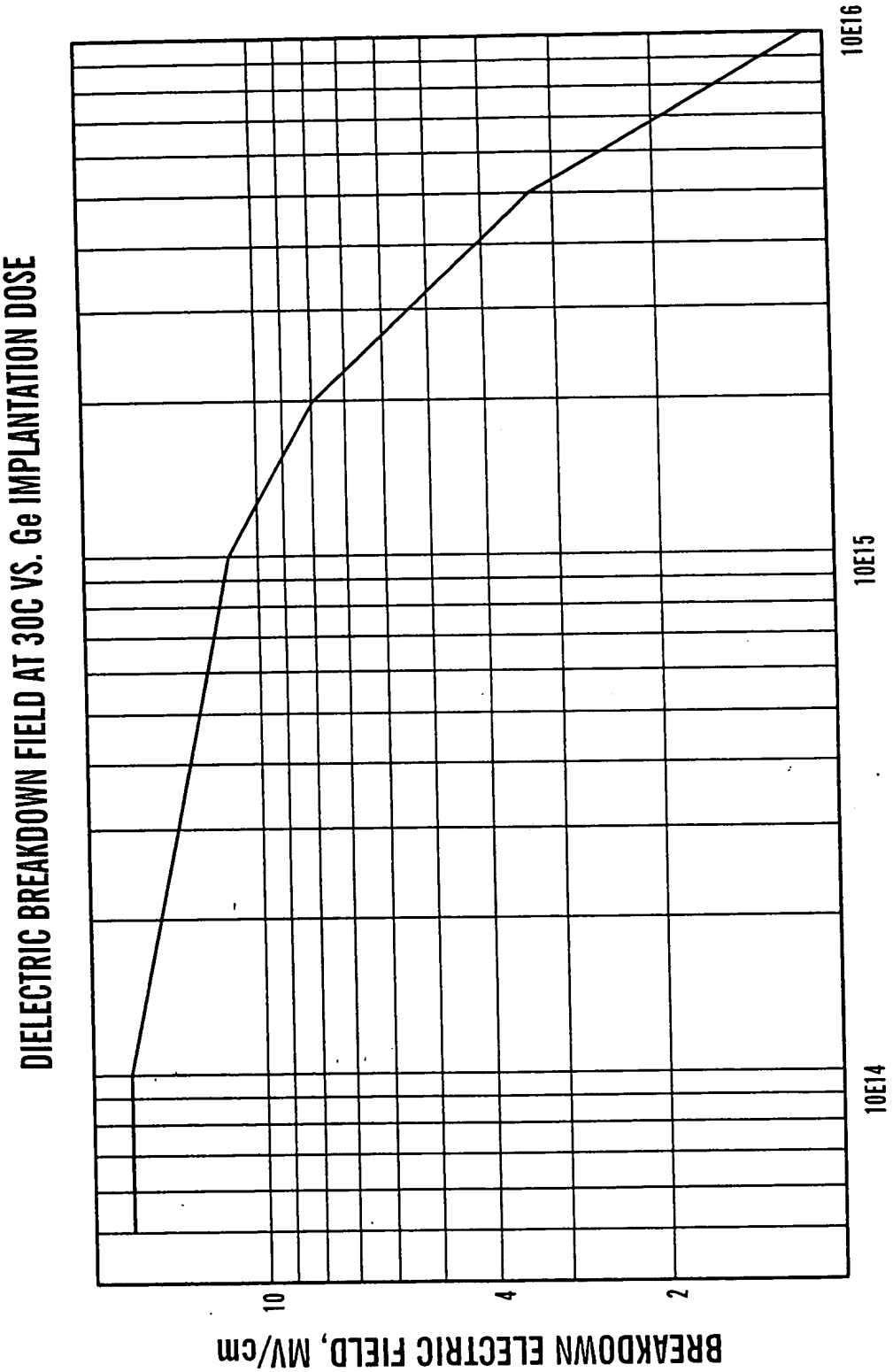
DIELECTRIC BREAKDOWN FIELD AT 30C VS. Ge IMPLANTATION DOSE
BREAKDOWN ELECTRIC FIELD, MV/cm
10
4
2
10E14
10E15
10E16
Ge IMPLANTATION DOSE, 1/cm2

FIG. 17

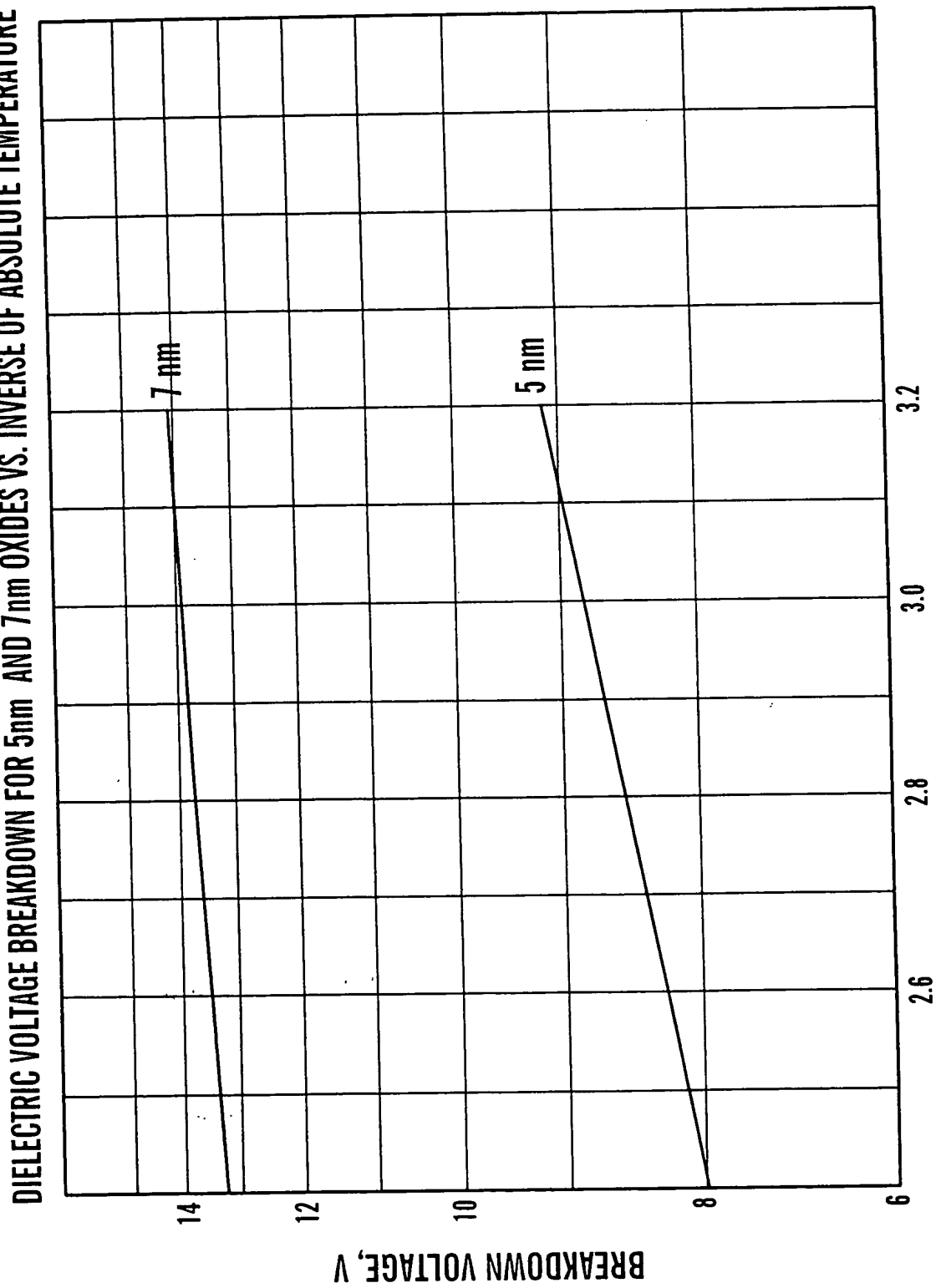
DIELECTRIC VOLTAGE BREAKDOWN FOR 5nm AND 7nm OXIDES VS. INVERSE OF ABSOLUTE TEMPERATURE
7 nm
5 nm
BREAKDOWN VOLTAGE, V
14
12
10
8
6
2.6
2.8
3.0
3.2
1000/T (1/K)

FIG. 18

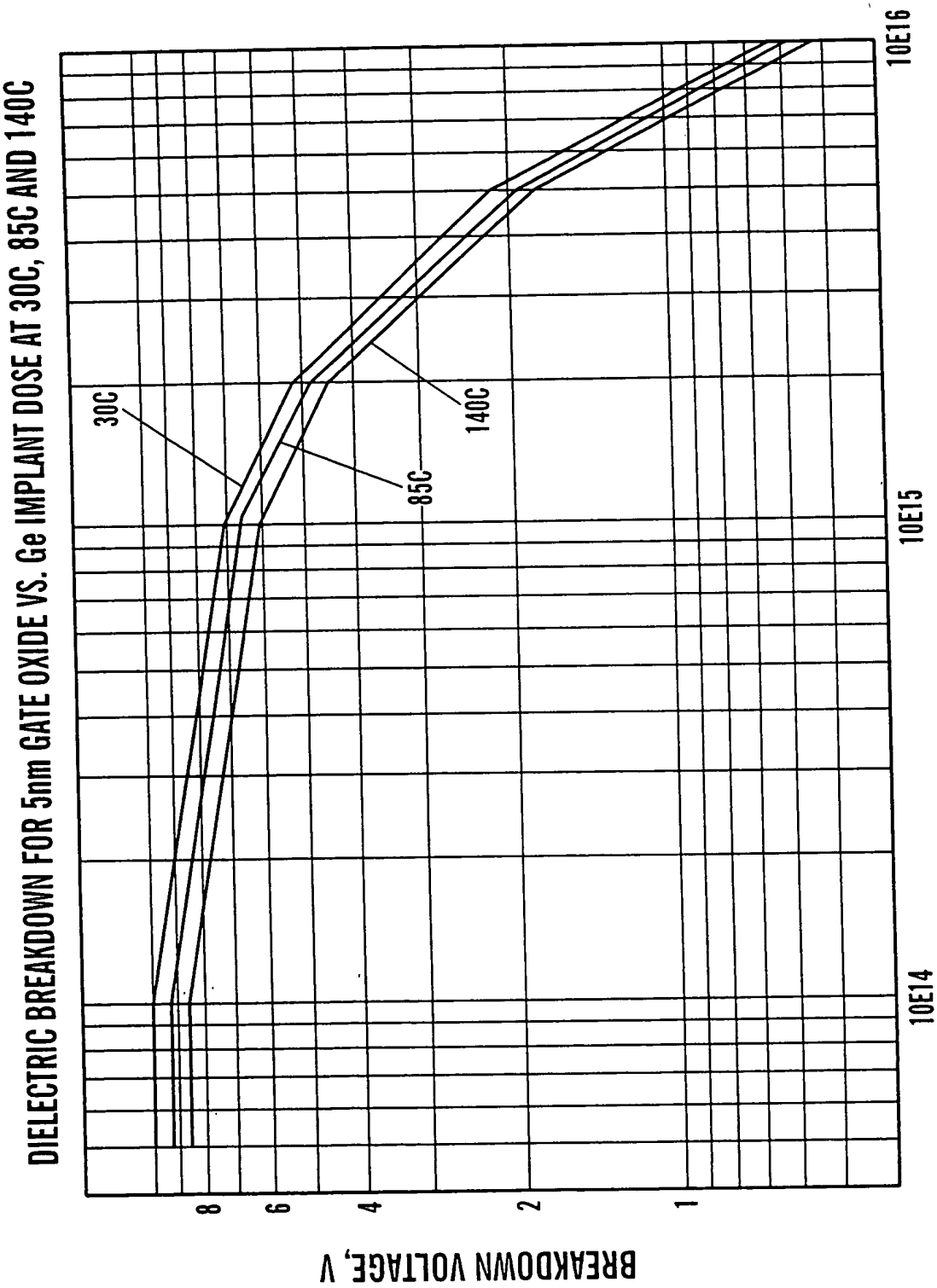
DIELECTRIC BREAKDOWN FOR 5nm GATE OXIDE VS. Ge IMPLANT DOSE AT 30C, 85C AND 140C
BREAKDOWN VOLTAGE, V
8
6
4
2
1
30C
85C
140C
10E14
10E15
10E16
Ge IMPLANTATION DOSE, 1/cm2

FIG. 19